AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A thin film transistor substrate in a liquid crystal display provided with a data line for applying a data signal, a gate line for applying a gate signal, and a pixel electrode for driving a liquid crystal cell, said substrate comprising:

a gate dummy pattern formed ~~so as to extend~~ vertically ~~from~~ to the gate line ~~and to overlap with the data line and the pixel electrode, the gate dummy pattern being integrated with the gate line~~, wherein the gate dummy pattern is formed to overlap with at least one of edge portions of the data line and an edge portion of the pixel electrode.

2. (Canceled)

3. (Currently Amended) The thin film transistor substrate according to claim ~~2~~ 1, wherein when the data line is broken, the gate dummy pattern is used as a redundancy electrode for electrically connecting ~~the gate line to~~ the broken data line.

4. (Currently Amended) The thin film transistor substrate according to claim 3, wherein the gate dummy pattern is formed to extend integratedly from the

gate line, and the gate dummy pattern includes a recess formed to permit a repair by disconnection of the gate dummy pattern from the gate line.

5. (Original) The thin film transistor substrate according to claim 1, wherein the gate dummy pattern is used as a black matrix.

6. (Original) The thin film transistor substrate according to claim 1, further comprising:

a storage capacitor defined by a horizontal overlapping part between the gate line and the pixel electrode.

7. (Previously Presented) The thin film transistor substrate according to claim 4, further comprising:

a protrusion protruded from the data line formed in such a manner as to overlap with the recess, thereby shutting off a light leaked between the gate dummy pattern and the gate line.

8. (Currently Amended) The thin film transistor substrate according to claim 1, ~~wherein the gate dummy pattern is formed on the lower substrate at each side of the data line,~~ wherein a gate-insulating layer is formed between the gate dummy pattern and the data line.

9. (Currently Amended) The ~~thin film~~ thin film transistor substrate according to claim 4, wherein the recess is provided at a cutting part for breaking the gate dummy pattern from the gate line in such a manner that the recess is not overlapped with the data line.

10. (Currently Amended) A thin film transistor substrate in a liquid crystal display provided with a data line for applying a data signal, a gate line for applying a gate signal, and a pixel electrode for driving a liquid crystal cell, said substrate comprising:

a gate dummy pattern formed ~~so as to extend~~ vertically ~~from~~ to the gate line and to overlap by ~~from~~ about 0.5-1 μm with at least one of the data line and an edge portion of the pixel electrode, to thereby serve as a black matrix to shut off light leaked between said data line and said pixel electrode~~, the gate dummy pattern being integrated with the gate line~~.

11. (Canceled).

12. (Currently Amended) The thin film transistor substrate according to claim ~~11~~ 10, wherein when the data line is broken, the gate dummy pattern is

used as a redundancy electrode for electrically connecting ~~the gate line to~~ the broken data line.

13. (Currently Amended) The thin film transistor substrate according to claim 12, wherein the gate dummy pattern is formed integratedly to extend from the gate line, and the gate dummy pattern includes a recess formed to permit a repair by disconnection of the gate dummy pattern from the gate line.

14. (Canceled)

15. (Previously Presented) The thin film transistor substrate according to claim 10, further comprising:

a storage capacitor defined by a horizontal overlapping part between the gate line and the pixel electrode.

16. (Previously Presented) The thin film transistor substrate according to claim 13, further comprising:

a protrusion formed in such a manner to overlap with the recess, thereby shutting off a light leaked between the gate dummy pattern and the gate line.

17. (Currently Amended) The thin film transistor substrate according to claim 10, ~~wherein the gate dummy pattern is formed on the lower substrate at each side of the data line,~~ wherein a gate-insulating layer is formed between the gate dummy pattern and the data line.

18. (Currently Amended) The ~~thin film~~ thin film transistor substrate according to claim 10, wherein the recess is provided at a cutting part for breaking the gate dummy pattern from the gate line in such a manner that the recess is not overlapped with the data line.

19-20. (Canceled)

21. (New) The thin film transistor substrate according to claim 1, wherein the gate dummy pattern is formed to cover mostly space between at least one of the edge portions of the data line and the edge portion of the pixel electrode.

22. (New) The thin film transistor substrate according to claim 6, wherein the gate dummy pattern is formed to extend integratedly from the gate line, and wherein an overlap portion of the gate dummy pattern and the edge portion of the pixel electrode with the gate insulating layer therebetween forms an auxiliary

storage capacitor.

23. (New) The thin film transistor substrate according to claim 10, wherein the gate dummy pattern is formed to cover mostly space between at least one of the edge portions of the data line and the edge portion of the pixel electrode.

24. (New) The thin film transistor substrate according to claim 15, wherein the gate dummy pattern is formed to extend integratedly from the gate line, and wherein an overlap portion of the gate dummy pattern and the edge portion of the pixel electrode with the gate insulating layer therebetween forms an auxiliary storage capacitor.

25. (New) A thin film transistor substrate for a display device including a data line extending in a first direction, a gate line extending in a second direction and crossing the data line, and pixel electrodes, the thin film transistor substrate comprising:

a gate dummy pattern including first and second extension parts extending from the gate line in the first direction and separated from each other, the first extension part disposed below a first edge portion of the data line and a side portion of an adjacent pixel electrode, the second extension part disposed below a

second edge portion of the data line and a side portion of another adjacent pixel electrode, the first and second edge portions being opposite edge portions of the data line.